Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-29 (Cancelled)

30. (Currently Amended) A ramping circuit assembly comprising:

an input port configured to receive ~~at least one~~ a plurality of decision feedback filter tap coefficients from a decision feedback filter, wherein the ~~at least one~~ plurality of decision feedback filter tap ~~coefficient is~~ coefficients are clamped;

a coefficient ramping circuit configured to provide a ramped output for ~~at least one of~~ the plurality of decision feedback filter tap coefficients, the ramped output being varied over time from a first value to a second value, the second value being dependent upon ~~a~~ respective tap coefficients of the plurality of decision feedback filter tap coefficients~~, wherein after the ramped coefficient have been ramped to approximately its full value, the decision feedback filter is configured to provide additional feedback filtering~~; and

an output port ~~coupled to a transmission channel and~~ configured to communicate information representative of the ramped output to a precoder ~~via the transmission channel~~ having a plurality of tap coefficients being ramped from an initial

value to a final value, wherein when the plurality of tap coefficients of the precoder reach their final value, the corresponding tap coefficients of the decision feedback filter will be at a corresponding final value of zero.

31. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

32. (Currently Amended) The ramping circuit assembly as recited in claim 30, wherein the information representative of the ramped first and second values comprises a difference between a present value of a tap coefficient of the precoder and a new value of the tap coefficient of the precoder.

33. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped generally linearly.

34. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped non-linearly.

35. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped generally exponentially.

36. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

37. (Cancelled)

38. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

39. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

40. (Currently Amended) A receiver comprising:

a feedforward filter including a plurality of feedforward filter taps, a feedforward filter reference tap, and a coefficient for each feedforward filter tap, wherein the reference tap is located proximate a center position of the feedforward filter and a value of the coefficient of the reference tap is greater than a value of each of the coefficients of each of the other feedforward filter taps;

a decision feedback filter in communication with the feedforward filter;

a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from the decision feedback filter, wherein the at least one decision feedback filter tap coefficient is clamped;

a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the ramped output being varied over time from a first value to a second value, the second value being

dependent upon the at least one of the decision feedback filter tap coefficients~~, wherein after the ramped coefficient have been ramped to approximately its full value, the decision feedback filter is configured to provide additional feedback filtering~~; and

an output port ~~coupled to a transmission channel and~~ configured to communicate information representative of the ramped output to a precoder ~~via the transmission channel~~.

41. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

42. (Currently Amended) The receiver as recited in claim 40, wherein the information representative of the ramped first and second values comprises a difference between a present value of a tap coefficient of the precoder and a new value of the tap coefficient of the precoder.

43. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped generally linearly.

44. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped non-linearly.

45. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped generally exponentially.

46. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

47. (Cancelled)

48. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

49. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

50.-59 (Cancelled)

60. (Currently Amended) A transceiver comprising:

a feedforward filter including a plurality of feedforward filter taps, a feedforward filter reference tap, and a coefficient for each feedforward filter tap, wherein the reference tap is located proximate a center position of the feedforward filter and a value of the coefficient of the reference tap is greater than a value of each of the coefficients of each of the other feedforward filter taps;

a decision feedback filter in communication with the feedforward filter

a precoder;

a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from the decision feedback filter, wherein the at least one decision feedback filter tap coefficient is clamped;

a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the ramped output being varied over time from a first value to a second value, the second value being dependent upon ~~a~~ the at least one decision feedback filter tap coefficient~~, wherein after the ramped coefficient have been ramped to approximately its full value, the decision feedback filter is configured to provide additional feedback filtering~~; and

an output port coupled to a transmission channel and configured to communicate information representative of the ramped output to a precoder of a complimentary transceiver via the transmission channel.

61. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

62. (Currently Amended) The transceiver as recited in claim 60, wherein the information representative of the ramped first and second values comprises a difference between a present value of a tap coefficient of the precoder of the complimentary transceiver and a new value of the tap coefficient of the precoder of the complimentary transceiver.

63. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped generally linearly.

64. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped non-linearly.

65. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped generally exponentially.

66. (Original) The transceiver as recited in claim 60, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

67. (Original) The transceiver as recited in claim 60, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

68.-97 (Cancelled)